Negative-R Assisted Integrator Based CT Delta-Sigma Modulator

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ABSTRACT

This paper presents third-order continuous-time delta-sigma modulator with topology of cascade of integrator with multiple feedforward (CIFF) having single-bit quantizer. The modulator noise transfer function (NTF) and signal transfer function (STF) calculated with reference to out-of-band A Negative-R based integrator implemented with operational amplifier to enhance the noise and linearity performance of the analog-to-digital converter. As these non-idealities degrades the performance and consume a lot of power that why a Negative-R assisted integrator utilized. The Negative-R assisted integrator on the front-end integrator used to minimize the operational amplifier performance parameters such as DC gain, unity gain bandwidth (UGB), thermal noise and linearity. This will reduce the power consumption due to use of Negative-R Assisted integrator. The modulator with Negative-R integrator can achieve signal-to-noise-plus-distortion (SNDR) and signal-to-noise-ratio (SNR) 86 dB and 86 dB respectively. The sampling frequency of the modulator is 10 MHz with oversampling ration (OSR) of 200 for the signal bandwidth of 25kHz. The modulator consumes power of 23 µW from 1-V supply.

Keywords: Negative-R, STF, NTF, OBG, Delta-Sigma.

1. INTRODUCTION

A 3rd-order single-bit delta-sigma modulator is modeled and simulated for hearing signals. The modulator can achieve 14-bit resolution with an oversampling ratio of 200. The complete modulator circuit non-idealities like limited DC gain, limited slew-rate, thermal noise, and flicker noise, modeled and simulated. A continuous-time delta-sigma modulator (CTDSM) is attractive as it offers several features including an intrinsic anti-aliasing filter, relaxed speed requirement of the op-amps, and a low-power consumption. Because a CTDSM's noise and linearity performance is determined by the first integrator, it is unavoidable that the first integrator will use a lot of power to meet the goal noise and linearity. Designing a low-power CTDSM without sacrificing its noise and linearity is therefore a difficult issue. The energy efficiency of CTDSMs has been improved by the investigation of many implementations in recent years. A multi-bit quantizer has largely been employed to relax the linearity requirements of the first integrator by reducing the step size of the feedback digital-to-analog converter (DAC) signal. However, a mismatch in unit elements of the feedback DAC limits the linearity performance of the CTDSM and requires dynamic element matching (DEM) which increases the power consumption and design complexity. On the other hand, a single bit quantizer, where the feedback DAC is inherently linear, simplifies the design and reduces the power consumption. In this paper, we propose

the negative-R assisted integrator, which is an active-RC integrator whose virtual ground is compensated by a negative resistor. The concept of compensating for a closed-loop op-amp with a negative resistor at its virtual ground was first proposed in to make the bandwidth of the op-amp infinite. We apply the concept to an active-RC integrator which is the most used in the loop filter of a CTDSM. The negative-R assisted integrator offers many advantages in the design of CTDSM that have not been reported before. The negative-R assisted integrator significantly relaxes the op-amp specifications such as the dc gain, unity gain bandwidth (UGB), noise, and linearity. Particularly, the noise of the op-amp including thermal and 1/f noise is attenuated and the distortion of the integrator is cancelled, thus leading to dramatic power savings.

2. NEGATIVE-R ASSISTED INTEGRATOR WORKING

The Negative-R Assisted integrator circuit used at the virtual ground of VG to provide path for VG and cancel Iloss current. The Fig. 1(a) shows the operation of an active-RC integrator. The finite response of an opamp A(s) makes the virtual ground non-ideal (VG = 0) and causes a current loss Iloss. As a result, the integrating current I_{INT} ($= I_{IN} - I_{loss}$) has the loss in its magnitude and bandwidth due to the finite gain and bandwidth of the op-amp, thus resulting in a lossy integrator. On the other hand, Fig. 1(b) shows the operation of the negative-R assisted integrator. When a negative-R is applied at the virtual ground, a compensation current Icomp is generated from the ground to cancel out Iloss and effectively makes the virtual ground ideal (VG = 0). Therefore, Iloss in the integrator caused by the finite gain and bandwidth of the op-amp is compensated and I_{INT} becomes equal to the input current I_{IN}.

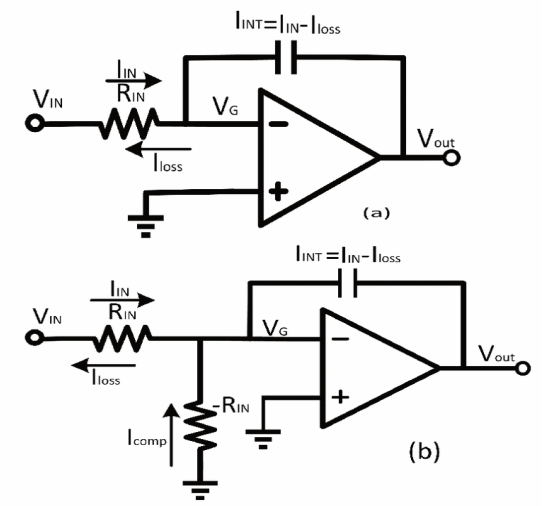

Figure 1: (a) Active RC (b) Negative-R

3. NEGATIVE-R ASSISTED INTEGRATOR CIRCUIT

The Negative-R Assisted Integrator circuit is cross-coupled double inverter circuit used before the amplifier is shown below. The Negative-R assisted integrator circuit relax the operational amplifier such as linearity, dc gain, unity gain bandwidth (UGB) decrease noise and reduce the power consumption of the op-amp.

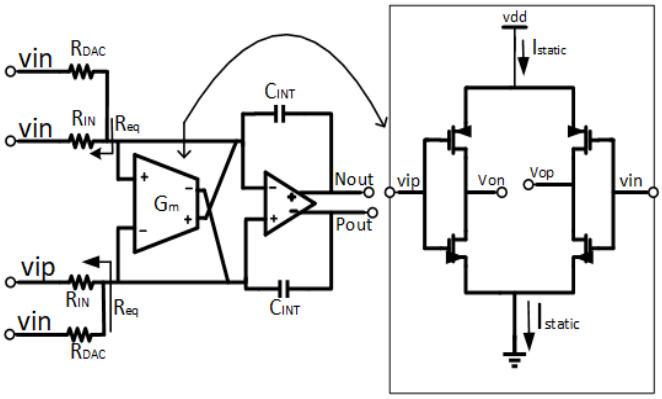

Figure 2: Negative-R Assisted Integrator

4. NEGATIVE-R WITH DELTA-SIGM

The delta-sigma because it includes an anti-aliasing filter ,a relaxed speed requirements for the operational amplifier, and low power consumption. The noise and linearity efficiency by using the first integrator. In order to generate the desired noise and linearity, the first integrator must use a lot of energy. Therefore, developing a low-power CTDSM is crucial, and the noise-free and linearity is a complicated process. The delta-sigma ADC is made up of a digital filter and a delta-sigma modulator. The modulator converts the analog input into a bit stream of digital data. The digital filter transforms the bit stream into a data word that corresponds to the magnitude of the analog input. A third-order delta-sigma modulator that the design are using three integrator,1-bit comparator,1-bit DAC and for power consumption reduction using negative resistance circuit. The different topology can be used in delta-sigma modulator. Now the design discuss the Cascode-integrator and feed-forword(CIFF) topology.

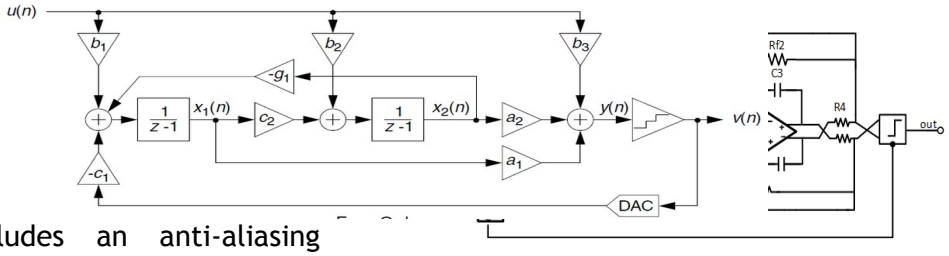

Figure 4: Block diagram of the CIFF topology

Figure 3: Delta-Sigma with Negative-R

5. CIFF TOPOLOGY

This paper proposed a cascade of integrator with multiple feedforward (CIFF) 3rd-order single-bit delta-sigma modulator. Both NTF and STF of the modulator use for higher performance. The NTF zero opt technique is used to remove in-band quantization noise to improve the performance. The (OBG) mean out of band gain of 2 selected for better noise shaping performance. The zeroes and poles effect of the NTF are discussed for accurate noise shaping. The zeroes of the NTF, which are poles of the loop filter needs to be at the DC on the unit circle without NTF zero optimization technique. The modulator can achieve higher performance by NTF zero optimization technique. The poles of the NTF, which are zeros of the loop filter lies inside the unit circle. The operational amplifier inside the loop filter optimized for higher performance. The non-idealities factors of the operational amplifier like limited DC gain modeled and simulated, as that causes the performance degradation. The

limited slew-rate also causes the harmonic distortion. Also, complete modulator non-idealities like thermal noise and flicker noise also modeled and simulated. The second-order modulator with an oversampling ration (OSR) of 200 easily can achieve signal to noise ratio (SNR) of 86 dB as with full-scale input of 500 mV. After the introduction, the second section discuss the design of the modulator with CIFF topology, while the third section describes the modeling and simulation of the modulator and explain the operation of the 3rd-order single bit. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

A modulator with CIFF topology and single-bit quantization is modeled using Delta-Sigma Toolbox [7] as shown in Figure 1. Due to CIFF topology the signal-transfer-function (STF) will have peaking issues but we have advantage of low-power operational amplifier can be used for integrator such as the signal swing inside the loop filter is small. The CIFF second-order modulator with NTF zero optimization technique can achieve signal to noise ratio of 86 dB with OSR of 200 with an OBG of 2. The modulator with CIFF topology coefficients is obtained from the Delta-Sigma Toolbox [18] shown in Table-I. The b_1 is the coefficient at the input while b_3 is the coefficient in front of quantizer. The modulator feedback coefficient is c_1, while c_2 is the interstage coefficient. The NTF zero optimization technique is implemented between the second integrator output to the input of first integrator. The Table II shows the OSR versus SNR comparison, different plot. It is shown clearly that higher OSR will results in increased SNR. Figure 7 shows the NTF and STF plot with NTF zero optimization technique implemented shown. The STF clearly shows the peak effect with low-pass filter response such as the modulator is low-pass. While the NTF shows the high pass filter response. The NTF response shows the quantization noise reduction from the signal band. The Figure 5 shows the output PSD plot for the modulator with OSR of 200 having SNR of

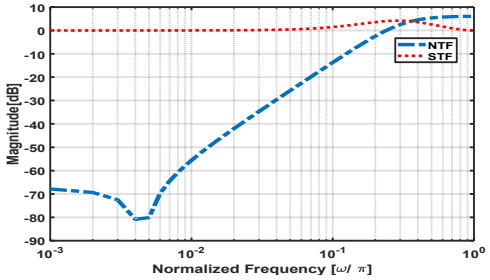

Figure 5: Output PSD plot (CIFB)

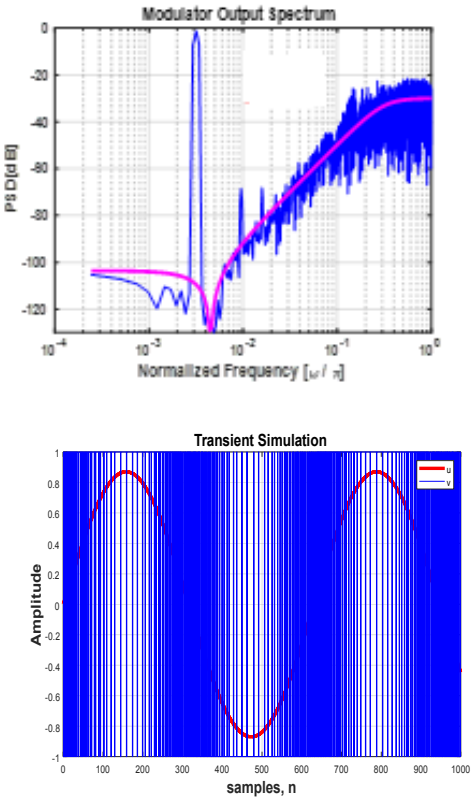

Figure 6: Transient response

Figure 7: STF and NTF plot (CIFF)

86 dB. The harmonic distortion can be seen very clearly in the output spectrum. The harmonic distortion is out-of-band which mean it does not contribute for the signal band performance. The Figure 6 shows the transient output response, that shows pulse coded modulation (PCM) output. This also shows the noise shaping behavior is working inside the loopfilter. The operational amplifier inside two integrator assumed infinite DC gain, and higher slew-rate. This causes maximum quantization noises attenuation.

1. NONIDEALITIES SIMULTION

1. Table I : CIFF Topology Cofficients

2. Parameters	3. Values
4. a1	5. 0.7998
6. a2	7. 0.7998
8. a3	9. 0.2880
10. b1	11. 1
12. b2	13. 0
14. b3	15. 0
16. c1	17. 1
18. c2	19. 1
20. c3	21. 1

22.

23. Table II: Results

24. parameter	25. values
26. OSR	27. 200
28. Bandwidth(kHz)	29. 25
30. SNR(dB)	31. 86
32. SFDR(dB)	33. 71

To realize the practical circuit implementation the modulator also simulated for circuit non-idealities like limited DC gain, limited slew-rate, these circuit non-idealities are simulated using SD Toolbox [8]. The thermal noise, flicker noise and limited DC gain also simulated. The simulation shows the degraded performance as compared to the actual ideal simulated modulator performance parameters.

4. CONCLUSION

The integrator with negative-R assisted that low-power audio-band CTDSM use to attain reducing energy efficiency and relax the op-amp requirements is described in this work. The operational amplifier in the CTDSM have noise and linearity issue. A continuous-time Delta-Sigma modulator have an op-amp, which (CTDSM) consume a lot of power. In order to reduce the requirements of op-amps. A negative-R assisted Integrator is studied that addresses several issues, including linearity, thermal noise, 1/f noise, and dc gain. This save a significant power decrease.

5. ACKNOWLEDGMENT

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